regions which typically occurs in prior art SiGe heterojunction bipolar transistors" and therefore is a permanent component of the structure depicted in FIG. 2. New Claim 18 clearly and positively recites that the passivation layer is deposited onto an "inclined portion" of the SiGe base region. Support for this amendment is found in FIG. 2 and FIG. 8.

Since the above amendments to the claims do not introduce any new matter into the application, entry thereof is respectfully requested. As required by 37 C.F.R. §1.121, applicants have attached a marked-up copy of Claims 1 and 9. The attachment is captioned as "MARKED UP VERSION SHOWING CHANGES MADE".

In the Final Rejection, Claims 1-17 were rejected under 35 U.S.C. §103(a) as allegedly obvious over the combination of applicants' admitted prior art ("AAPA") in view of U.S. Patent No. 5,936,189 to Tsuchiaki ("Tsuchiaki") and further in view of ADEL S. SEDRA & KENNETH C. SMITH, MICROELECTRONIC CIRCUITS (4TH Ed 1998)("Sedra and Smith"). Applicants respectfully submit that the §103 rejections have been obviated in light of amendments to Claim 1, Claim 9, and newly added Claim 18.

Applicants submit that Claims 1-17, and new Claim 18, of the present application are not obvious from the applied references or the AAPA since none of the references teaches or suggests applicants' claimed method or structure which includes providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in the insulator layer. A permanent conformal passivation layer is then formed on the exposed sidewalls of the emitter, insulator layer,

and a portion of the SiGe base regions. The exposed silicon regions not covered by the permanent conformal passivation layer are then silicided. The referenced prior art also fails to teach or suggest applying the permanent conformal layer onto the inclined portion of the SiGe base region, as recited in new Claim 18.

Applicants submit that the primary reference, the AAPA as depicted in FIG. 1, fails to teach or suggest a permanent conformal passivation layer. The AAPA discloses a heterojunction bipolar transistor structure, which does not incorporate the conformal passivation layer. The heterojunction bipolar transistor structure as disclosed in the AAPA typically results in a 20-30% bipolar yield loss. The loss associated with the SiGe bipolar transistor structure, as disclosed in the AAPA, is attributed to the presence of silicide bridges between the emitter and SiGe body, which introduce shorts to the structure during silicidation. Applicants' claimed method and structure utilize a permanent conformal passivation layer to avoid the formation of silicide bridges and losses associated with prior art devices.

The above deficiencies in the AAPA are not alleviated by the disclosure of Tsuchiaki since the applied reference does not teach or suggest a final device structure including a permanent conformal passivation layer positioned on the exposed sidewalls of an emitter, a patterned insulator layer and a portion of a SiGe base region; and silicide regions which are located on exposed portions of a SiGe layer, including portions of the SiGe base region and the emitter not covered by the permanent conformal passivation layer.

Applicants submit Tsuchiaki fails to teach or suggest a final SiGe bipolar transistor structure incorporating a permanent conformal passivation layer, wherein the

permanent conformal passivation layer decreases the incidence of silicide bridges by protecting the surfaces underlying the passivation layer from being silicided. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art" In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Tsuchiaki provides a temporary passivation layer that is only utilized as an etch stop in the formation of a MOSFET device. Once the etch steps have been completed, the temporary passivation layer is removed and consequently does not remain as a structural component of the final device. Therefore, Tsuchiaki does not teach or suggest all of the limitations of the applicants' final structure recited in Claim 9.

Additionally, Tsuchiaki does not teach or suggest silicide formation or the use of a passivation layer during silicide formation and therefore fails to teach or suggest all of the limitations of applicants' method as recited in Claim 1. Claim 1 recites forming a permanent passivation layer on said exposed sidewalls of said emitter, said insulator layer and portions of said SiGe base; and siliciding exposed Si surfaces of at least said emitter and said SiGe base region not protected by said permanent passivation layer to form silicide regions therein. Tsuchiaki only discloses using the temporary passivation layer as an etch stop barrier and therefore does not teach or suggest siliciding the exposed Si containing surfaces, of the emitter and the SiGe body, not underlying a permanent conformal passivation layer as recited in Claim 1. Therefore, Tsuchiaki fails to teach or suggest applicants' method.

Referring to new Claim 18, Tsuchiaki fails to teach or suggest a permanent conformal passivation layer applied to an inclined surface of a SiGe base region, as

recited in Claim 18. Tsuchiaki discloses forming a temporary passivation layer **204** on the vertical sidewalls of island structures **203** and does not teach or suggest forming passivation layers on inclined surfaces as recited in new Claim 18. Tsuchiaki referring to Column 6, lines 38 – 44, disclose that "thin passivation layers **204** are formed on the sidewalls i.e., vertical planes of the island structure because the vertical planes are free from ion impingement. On the other hand, at the horizontal bottom surface of the substrate **205**, ions impinging vertically from plasma onto the substrate prevent the formation of passivation layers on this surface (the horizontal surface)." Therefore, Tsuchiaki does not teach or suggest forming a passivation layer on to an inclined surface of a SiGe base region, as recited in Claim 18.

Tsuchiaki as a whole teaches away from applicants' invention. "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Tsuchiaki, referring to Column 7, line 5, specifically teaches a temporary passivation layer for the purpose of an etch stop during a selective etch step, where after the etch step is concluded the temporary passivation layer is removed, therefore teaching away from applicants' claimed structure comprising a permanent passivation layer that remains in the final structure of the device. Tsuchiaki teaches away from applicants' method and structure recited in Claims 1 and 9.

Sedra and Smith, do not fulfill the deficiencies of the AAPA and the Tsuchiaki reference. Sedra and Smith, referring to page 222, disclose a bipolar junction transistor consisting of three semiconductor regions; the emitter, the base region, and the collector

region. Sedra and Smith fail to teach or suggest a permanent conformal passivation layer as recited in amended Claims 1 and 9 and new Claim 18.

The §103 rejection also fails because there is no motivation to modify the prior art structures to include applicants' claimed method and structure, where a permanent passivation layer defines the locations where silicide regions contact the SiGe layer and surface of the emitter, as recited in Claims 1 and 9. Additionally, the referenced prior art fails to provide motivation to apply the permanent conformal passivation layer to the inclined surfaces of the SiGe base region, as recited in new Claim 18. The §103 rejection is thus improper since the prior art does not suggest this dramatic modification.

The law requires that a prior art reference provide some teaching, suggestion or motivation to make the modification. In re Vaeck, 947 F.2d 488, 493, 20 USPQ 2d 1438, 1442 (Fed. Cir. 1991). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. "In re Fritch, 972 F.2d 1260, 1266, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992).

Referring to page 5 of the previous Final Rejection, the Examiner contended that the suggestion to combine the above references is that it is within the knowledge generally available to one of ordinary skill in the art to remove the silicide regions and replace them with a passivation region in the joint areas of the emitter and base in order to further isolate the emitter and the base contacts so there would be no shorts between base and emitter.

A statement that modifications of the prior art to meet the claimed invention would have been " ' well within the ordinary skill of the art at the time the claimed

invention was made' " because the references relied upon teach all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima fascia case of obviousness without some objective reason to combine the teachings of the references. Ex Parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. and Inter. 1993).

Applicants submit that the Examiner has gleaned knowledge from applicants' disclosure to provide an objective reason for combining the AAPA with the above references to include the structure and method recited in Claims 1 and 9. The teaching or suggestion to make the claimed combination must be found in the prior art and not based on applicant's disclosure. See In re Vaeck, 947 F.2d 488, 20 USPQ 2d 1438 (Fed. Cir. 1991).

First, a major problem with the prior art SiGe heterojunction bipolar transistors is that the SiGe bipolar yield is significantly reduced because of the presence of shorts which are introduced into the structure during the silicide process. The shorts are caused by the presence of silicide bridges that exist in the structure. As such, a 20-30% yield loss is typically associated with prior art SiGe heterojunction bipolar transistors. Applicants' inventive method and structure have alleviated the above by incorporating a permanent conformal passivation region, which does not allow the formation of silicide bridges. Applicants' disclosure is the only teaching for utilizing a permanent passivation layer in a manner that would alleviate shorting during silicidation and silicon bridge formation.

Second, as discussed above, the AAPA and Sedra and Smith do not teach or suggest a permanent conformal passivation layer. The temporary passivation layer disclosed in Tsuchiaki is removed before the structure of the device is completed and it

utilized for a totally different purpose than the conformal passivation layer recited in the applicants' claims. Additionally, Tsuchiaki teaches away from applicants' invention because it discloses the passivation layer as an etch stop that is removed before device finalization and does not address silicidation or shorting due to silicide bridge formation. Further, none of the applied references addresses silicide formation, or more importantly reducing the silicide bridge formation. The applied references do not teach or suggest incorporating a permanent conformal passivation layer as recited in amended Claims 1 and 9.

Applicants respectfully submit a prima facie case of obviousness based on modifications being well within the ordinary skill of the art can not be supported by the objective reasoning to combine the teachings because the Examiner has impermissibly gleaned the objective reasoning to combine the applied references from the applicants' disclosure. "A piecemeal reconstruction of the prior art patents in the light of the applicants' disclosure shall not be the basis for a holding of obviousness." In re Rothermel, 47 CCPA 866, 276 F.2d 393, 396, 125 U.S.P.Q. 328, 331 (1960). "It is impermissible within the framework of §103 to pick and choose from any one reference only as much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggest to one of ordinary skill in the art". In re Wesslau, U.S.P.Q. 391, 393 (1965).

There is no suggestion in the prior art of applicants' claimed method or structure recited in pending Claims 1-17 and new Claim 18. As such, the claims of the instant application are not obvious from any of the above-mentioned prior art references.

Therefore, applicants respectfully submit that the rejection under 35 U.S.C. §103 has been obviated; and the withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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MARKED UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please amend Claim 1 and Claim 9 as follows:

1. (Twice amended) A method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar transistor comprising the steps of:

providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls;

forming a permanent passivation layer on said exposed sidewalls of said emitter, said insulator layer and portions of said SiGe base region; and

siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said permanent passivation layer to form silicide regions therein.

9. (Three times amended) A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and a portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer.

Please add new Claim:

--18. A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a permanent conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and an inclined portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said permanent conformal passivation layer.--